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**Research Paper**

# Comparator Design Using Various Full Adder Designs.

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**Abstract:** In this paper a new design of comparator is described with the help of Full adder which are the basic building block of ALU and ALU is a basic functioning unit of the microprocessors and DSP. In the world of technology it has become essential to develop various new design methodologies to reduce the power and area consumption. In this paper comparator is developed using various designs of full adder. The proposed one will reduce the power of the comparator remarkably. The proposed comparator has been designed using DSCH 3.1 and Micro wind 3.1 at 32nm technologies. In proposed comparator power dissipation is reduced from micro Watts to Nano Watts and almost 50 % of area reduction is achieved.

**Key Words:** Full adder, NMOS, PMOS, CMOS, speed, low power, less transistor count, efficiency.

## 1. Introduction

The Comparator is a very basic and useful arithmetic component of digital systems. There are several approaches to designing CMOS comparators, each with different operating speed, power consumption, and circuit complexity. One can implement the comparator by flattening the logic function directly **[1]-[6].** Full adder is one of the basic building blocks of many of the digital VLSI circuits. Several refinements have been made regarding its structure since its invention. The main aim of those modifications is to reduce the number of transistors to be used to perform the required logic, reduce the power consumption and increase the speed of operation. One of the major advantages in reducing the number of transistors is to put more devices on a single silicon chip there by reducing the total area. One of the ways to reduce power is to explore new types of circuits in order to find better circuit techniques for energy savings. In this paper, we propose several design techniques for high performance and power efficient CMOS comparators. Here we use Micro wind to draw the layout of the CMOS circuit. In digital system, comparison of two numbers is an arithmetic operation that determines if one number is greater than, equal to, or less than the other number **[7]-[12].**So comparator is used for this purpose. Magnitude comparator is a combinational circuit that compares two numbers, A and B, and determines their relative magnitude. The outcome of comparison the outcome of comparison is specified by three binary variables that indicate whether B>A, A=B. Full adder based comparator is a 2-bit comparator consist of 2 full adders, 2 inverters at one of the input and 2 AND gates at the output side. There are two outputs. One shows A=B and another shows B>A .Truth table of full adder based comparator is as shown in figure 1.

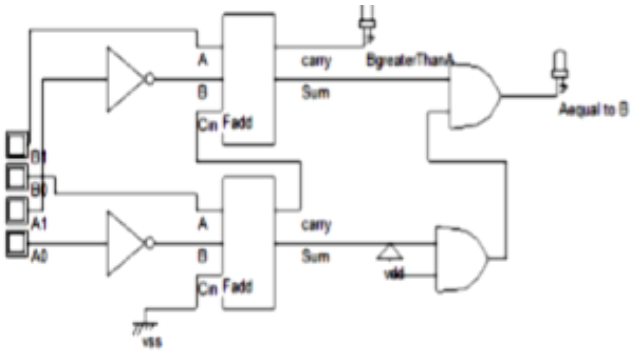


*Figure - 1: full adder based 2-bit comparator*

| A1 | A0 | B1 | B0 | B >A | A=B |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 0 | 1 | 1 | 0 |
| 0 | 0 | 1 | 0 | 1 | 0 |
| 0 | 0 | 1 | 1 | 1 | 0 |
| 0 | 1 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 0 | 0 |
| 1 | 0 | 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 | 1 | 0 |
| 1 | 1 | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 1 | 0 | 0 | 0 |
| 1 | 1 | 1 | 1 | 0 | 1 |

*Table - 1: Truth table of full adder based 2-bit comparator*

## 2. Literature Survey

A basic full adder has three inputs and two outputs which are sum and carry. The logic circuit of this full adder can be implemented with the help of XOR gate, AND gates and OR gates. The logic for sum requires XOR gate while the logic for carry requires AND, OR gates. The basic logic diagram for full adder using its Boolean equations with basic gates can be represented as shown below.

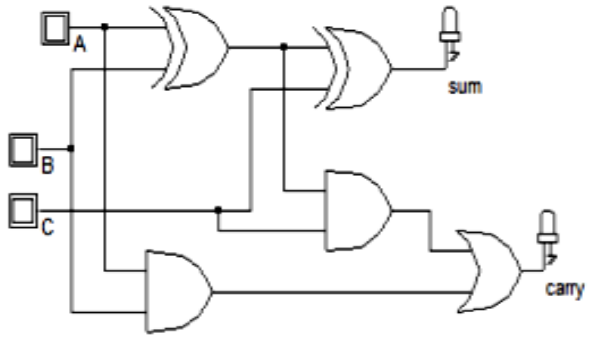


*Figure - 2: Logic diagram of basic full adder*

The XOR gate is the basic building block of the full adder circuit. The performance of the full adder can be improved by enhancing the performance of the XOR gate. Several refinements have been made in its structure in terms of transistors to increase the performance of full adder. The early designs of XOR gates were based on eight transistors or six transistors that are conventionally used in most designs. The main intention of reducing this transistor count is to reduce the size of XOR gate. So that large number of devices can be configured on a single silicon chip. There by reducing the area and delay.

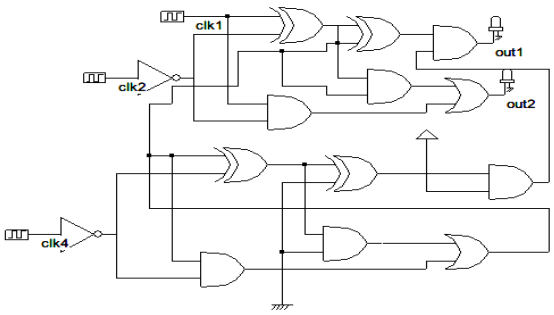


*Figure - 3: Logic diagram of basic full adder comparator*

The layout design of the basic full adder based comparator is shown in the figure 4. Layout is the general concept that describes the geometrical representation of the circuits by the means of layers. Different logical layers is used by designers to generate the layout.

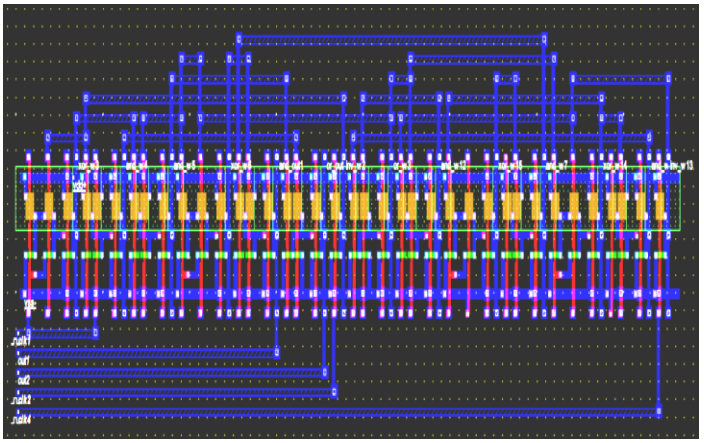

*Figure - 4: layout design of basic full adder based comparator*

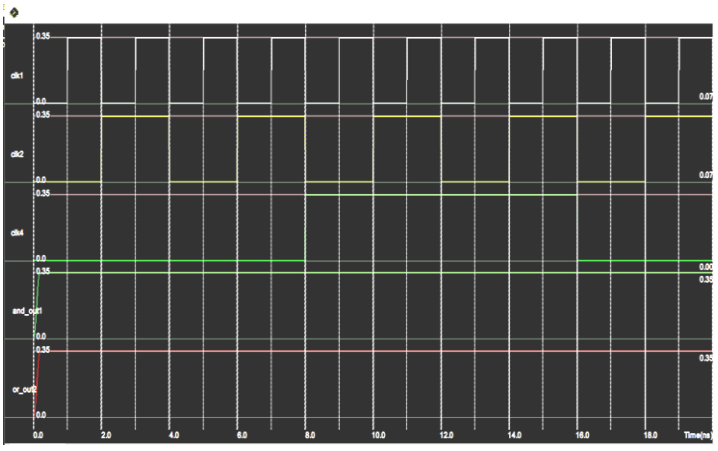

*Figure - 5: Simulation output of basic full adder based comparator*

The logic diagram of hybrid comparator is as shown below .This logic style consist of two XOR gate and one multiplexer.

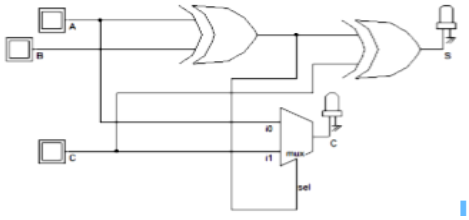

*Figure - 6: logic diagram of hybrid comparator*

The comparator using hybrid full adder is shown in figure 6.The comparator consumes more power and area as compared to the basic full adder based comparator. It consists of four XOR gate, two multiplexer, two NOT gate and two AND gates. Comparator has four input (A1, A0, B1, B0) and two output (A=B, B>A).

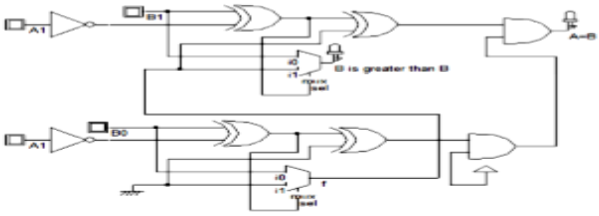

*Figure - 7: logic diagram of hybrid full adder based comparator*

The layout design of hybrid full adder based Comparator is shown in figure 7.

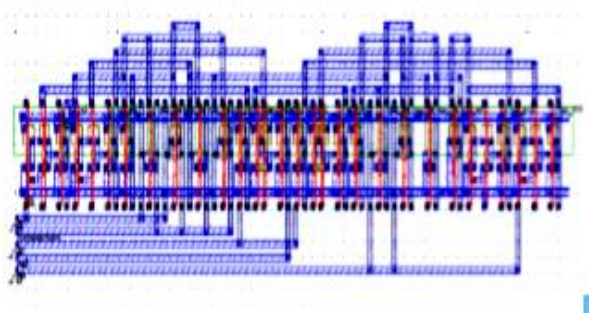

*Figure - 8: layout design of hybrid full adder based comparator*

## 3. Proposed work

Proposed work of comparator is based on another logic style of full adder. This logic style of comparator provides less power consumption than other logic styles described in this paper. The implementation of new logic full adder based comparator is shown in figure 9.It consists of two full adders, two NOT gates at one of the input and two AND gates at the output of the comparator. It has four input (A1, B1, A0, B0) and two output (A=B, B>A).

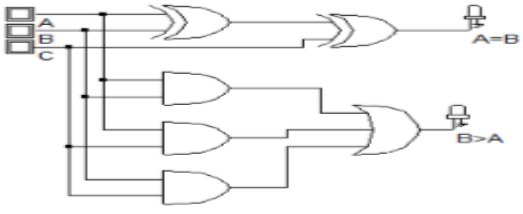


*Figure - 9: logic diagram of full adder using logic*

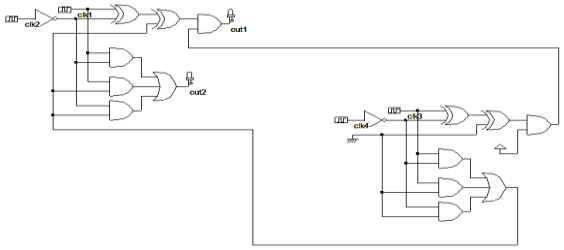

*Figure - 10: logic diagram of full adder based comparator*

The layout design of comparator using another logic of full adder is shown in figure 10. Layout is the general concept that describes the geometrical representation of the circuits by the means of layers and polygons. Different logical layers are used by designers to generate the layout.

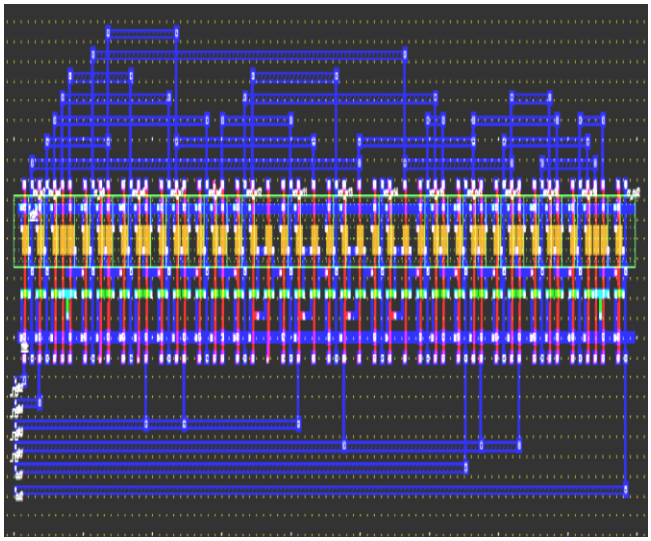

*Figure - 11: layout design of full adder based comparator*

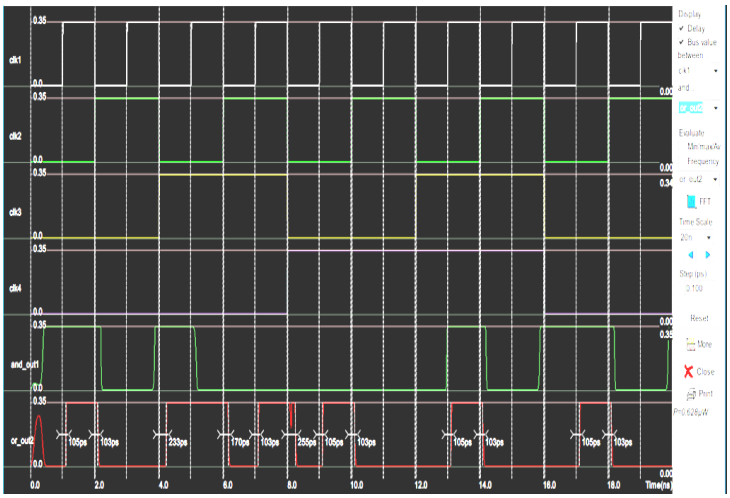


*Figure - 12: Simulation output of full adder based comparator*

The proposed comparator consists of XOR gate, MUX, NOT and AND gate with four input (A1, A0, B1, B0) and two output (A=B, B>A) as shown in figure 13.

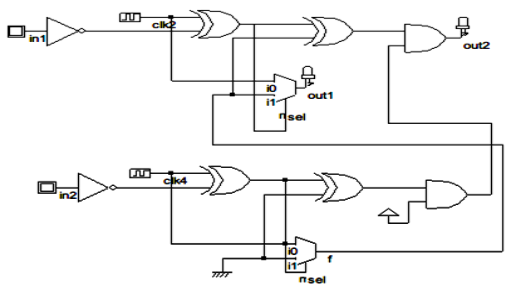


*Figure - 13: Proposed Hybrid Full Adder Based Comparator*

The layout design of the proposed hybrid full adder based Comparator is shown in figure 14 and its analog simulation in figure 15.

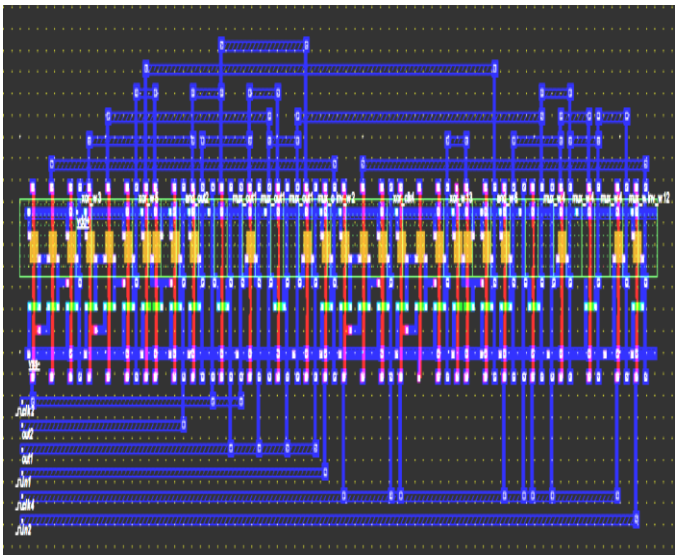

*Figure - 14: layout design of full adder based comparator*

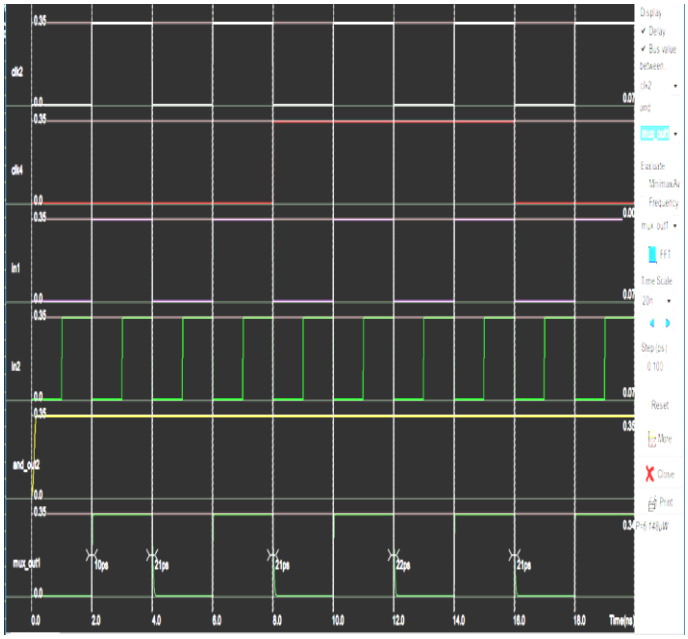

*Figure - 15: Simulation output of proposed full adder based comparator*

## 4. Result Analysis

Table 2 shows simulation output results of all logic styles. First step in obtaining the simulations is to compile the Verilog file in Micro wind 3.1. Verilog file is created from the circuit diagram, which is designed in the schematic. The Verilog file is now compiled in Micro wind 3.1. After the compilation of Verilog file, the layout for the circuit diagram drawn in schematic will be generated in Micro wind. After that simulations are performed on the layout generated using Verilog files. The results are simulated at room temperature.

*Table - 2: Simulation results of various full adder based comparator*

| | Power consumed | Area $\mu m^2$ | Memory usage in % | NMOS devices | PMOS devices | Electrical nodes |
|---|---|---|---|---|---|---|
| Basic full adder Comparator | 0.237 µW | 66.2 | 8.6 | 38 | 37 | 63 |
| Full adder based comparator | 0.628 µW | 43.2 | 9.9 | 46 | 46 | 53 |
| Hybrid full adder based comparator | 6.2 nW | 37.6 | 5.9 | 26 | 26 | 38 |

## 5. Conclusion

This paper describes different logic styles of full adder for designing a comparator for low Power Consumption. Basic full adder based comparator Logic Style provides low power and area design as compared to other Logic Style. Hybrid comparator logic style provides high power consumption and area. The proposed comparator consumes less power as compared to other logic styles. But the area consumption is greater than basic full adder based comparator. By using the proposed architecture the power is reduced up to 6.2nW and area is reduced up to 46% than the other logic styles.

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